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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/781,883
Filing Date: February 20, 2004
Appellant(s): SEAL ET AL.

John R. Lastova (Reg. No. 33,149)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/30/2008 appealing from the Office action mailed 10/22/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5459854	Sherer et al.	10-1995
6968444	Kroesche et al.	11-2005
5,781,753	McFarland et al.	7-1995
2004/0030856	Qureshi et al.	02-2004
20040059848	Chang et al.	03-2004

dictionary.com. "Definition for subset". 2 pages, 1900-2005 (depending upon the entry).

Roberts, H Edward. Yates, William. "Altair 8800". Pages 1-5, January 1975.

Claim Construction

In Appellant's independent claims (using Claim 1 as an example), it has been claimed that there is data processing logic configured to perform data processing operations. Given that this is the purpose of all computing machines, Examiner interpreted this limitation straightforwardly, based on the claim language. Since Qureshi teaches executing instructions, as all computers do, Examiner mapped Qureshi to this limitation in general, as Qureshi must comprise some data processing logic in order to perform the operations it clearly executes, as it is a computer.

Appellant further claims an instruction decoder, configured to decode program instructions. Since an instruction decoder is a required component for all processors, since instructions (or any data in a computer), for all intents and purposes, is a collection of jumbled up ones and zeros, until put into a proper context by a decoder, Examiner asserted, similar to the above data processing logic, that any computer would

have an instruction decoder, since it is fundamentally impossible to have a computer which executes instructions without a decoder. Since Qureshi executes instructions, it must have an instruction decoder.

Appellant further claims that there are instructions from a first instruction set, and instructions from a second instruction set. Examiner noted that there is no indication, explicit or implicit, in the claims that the instruction sets are different. Without any such indication, it could be interpreted that the instruction sets are different, however, it is also a valid interpretation that the first and second labels are simply used as identifiers. For example, one could claim a first and a second barrel. The first barrel could contain apples, and the second barrel could contain apples as well. Or the first barrel could contain apples, and the second barrel could contain oranges. In either case, the claiming of "a first barrel, and a second barrel" is proper. Therefore, the two proper interpretations of this limitation are that the instruction sets are the same, or that the instruction sets are different, and in order to make the broadest reasonable interpretation, as required by the MPEP, the Examiner interpreted that the limitation could be both. Since Qureshi read upon the instruction sets being the same, Examiner applied the art to the claims.

The Appellant further claimed that the first instruction set had a subset of instructions, that had a common storage order compensated encoding with a subset of instructions from the second instruction set, such that when all differences were accounted for, all bits were identical, and formed a common subset of instructions. Examiner interpreted this limitation by applying the dictionary definition of “subset”, as

the Appellant has provided no definition of subset, in either the claims or the specification. The Dictionary definition, attached to this action, shows that a subset is "a set that is part of a larger set", "a set consisting of elements of a given set that can be the same as the given set or smaller", and "a set whose members are members of another set", among other definitions. Given that a subset, when presented with the dictionary definition, can mean that either a smaller set than the entire set, or the entire set, Examiner used the broadest reasonable interpretation of the word, in correspondence with the MPEP, which is that all definitions of the word are reasonable. Qureshi read upon the claim where a subset is the whole set (that is, the first subset is equal to the second subset), and Examiner applied the reference. The remaining limitations require that when all storage differences were accounted for, all bits would be the same. Qureshi teaches that an instruction set can be stored in two different formats, and when you compensate for these two storage format differences, all bits are identical. Therefore, Examiner applied Qureshi to these limitations.

The remaining limitation of the claim states that this common subset of instructions controls the data processing logic to perform the same data processing operations, independent of the mode of the instruction decoder. Qureshi teaches that when the storage differences are accounted for, all bits are identical, thus an instruction stored in one format is identical to the same instruction stored in the second format, thus the exact same procedure would result, therefore Examiner applied the art to the claim.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6, 8-17, 19-28, and 30-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Qureshi et al. (United States Patent Application Publication 2004/00308856, herein Qureshi).

3. As per Claim 1, Qureshi teaches: An apparatus for processing data, said apparatus comprising:

data processing logic configured to perform data processing operations (Paragraph 13, this is what processors do); and

an instruction decoder configured to decode program instructions specifying data processing operations to be performed by said data processing logic and to control said data processing logic to perform said data processing operations (Paragraph 5, the decode logic); wherein

said instruction decoder is configured in a first mode in which program instructions of a first instruction set are decoded (Paragraph 5, little endian) and in a second mode in which program instructions of a second instruction set are decoded (Paragraph 5, big endian), a subset of program instructions of said first instruction set having a common storage order compensated encoding with a subset of program instructions of said second instruction set such that, after compensating for storage order differences, all bits are identical (See Tables 1 and 2 on pages 1 and 2 respectively) and forming a common subset of instructions representing at least one class of instructions (Paragraphs 14 and 16, the instructions are the same, just stored differently), said common subset of instructions controlling said data processing logic to perform the same data processing operations independent of whether said instruction decoder is operating in said first mode or said second mode (Paragraphs 14 and 16, the instructions are the same, just stored differently).

4. As per Claim 12, Qureshi teaches: A method of processing data, said method comprising the steps of:

performing data processing operations with data processing logic (Paragraph 13, this is what processors do); and

decoding with an instruction decoder program instructions specifying data processing operations to be performed by said data processing logic and controlling said data processing logic to perform said data processing operations (Paragraph 5, the decode logic); wherein

in a first mode program instructions of a first instruction set are decoded (Paragraph 5, little endian) and in a second mode program instructions of a second instruction set are decoded (Paragraph 5, big endian), a subset of program instructions of said first instruction set having a common bit-length and a common storage order compensated encoding with a subset of program instructions of said second instruction set such that, after compensating for storage order differences, all bits are identical (See Tables 1 and 2 on pages 1 and 2 respectively) and forming a common subset of instructions representing at least one class of instructions (Paragraphs 14 and 16, the instructions are the same, just stored differently), said common subset of instructions controlling said data processing logic to perform the same data processing operations independent of whether said instruction decoder is operating in said first mode or said second mode (Paragraphs 14 and 16, the instructions are the same, just stored differently).

5. As per Claim 23, Qureshi teaches: A computer program product having a computer program operable to control a data processing apparatus containing data processing logic operable to perform data processing operations (Paragraph 13, this is what processors do), said computer program comprising:

program instructions of a first instruction set (Paragraph 5, little endian) and program instructions of a second instruction set (Paragraph 5, big endian), that control said data processing logic to perform said data processing operations;

wherein a subset of program instructions of said first instruction set have a common bit-length and a common storage order compensated encoding with a subset of program instructions of said second instruction set such that, after compensating for storage order differences, all bits are identical (See Tables 1 and 2 on pages 1 and 2 respectively) and form a common subset of instructions representing at least one class of instructions (Paragraphs 14 and 16, the instructions are the same, just stored differently), said common subset of instructions controlling data processing logic to perform the same data processing operations independent of whether instructions of said first instruction set or of said second instruction set are being decoded (Paragraphs 14 and 16, the instructions are the same, just stored differently).

6. As per Claim 2, Qureshi teaches: The apparatus as claimed in claim 1, wherein said instruction decoder is operable to use common portions of said data processing logic to execute instructions of said common subset of instructions (Column 5, there is only one set of logic, which works regardless of the mode).

Claims 13 and 24 are substantially similar to Claim 2, and are rejected for the same reasons.

7. As per Claim 3, Qureshi teaches: The apparatus as claimed in claim 1, wherein said common subset of instructions includes a class of instructions being coprocessor instructions operable to control coprocessor data processing operations using

coprocessor logic common to said first instruction set and said second instruction set (Column 5, there is only one set of logic, which works regardless of the mode).

Claims 14 and 25 are substantially similar to Claim 3, and are rejected for the same reasons.

8. As per Claim 4, Qureshi teaches: The apparatus as claimed in claim 3, wherein all unconditional coprocessor instructions are within said common subset (Column 5, all instructions are in the subset).

Claims 15 and 26 are substantially similar to Claim 4, and are rejected for the same reasons.

9. As per Claim 5, Qureshi teaches: The apparatus as claimed in claim 1, wherein said first instruction set is a fixed length instruction set of N-bit instructions (Column 21).

Claims 16 and 27 are substantially similar to Claim 5, and are rejected for the same reasons.

10. As per Claim 6, Qureshi teaches: The apparatus as claimed in claim 5, wherein N is one of 32 or 16 (Column 21, it is 32 bits).

Claims 17 and 28 are substantially similar to Claim 6 and are rejected for the same reasons.

11. As per Claim 8, Qureshi teaches: The apparatus as claimed in claim 1, wherein at least one program instruction within said common subset of instructions performs common data processing operations in either said first mode or said second mode but generates different result data values depending upon whether said instruction decoder is operating in said first mode or said second mode (Paragraph 1, depending upon the order in which the data is presented, radically different results will result, as reading an instruction backwards will generate a very different answer as if you read it in the proper order).

Claims 19 and 30 are substantially similar to Claim 8 and are rejected for the same reasons.

12. As per Claim 9, Qureshi teaches: The apparatus as claimed in claim 8, wherein said at least one program instruction generating different result data values includes a program counter value as an input operand (Paragraph 1, if the machine is reading data in an order it wasn't intended to be read in, everything will generate different results).

Claims 20 and 31 are substantially similar to Claim 9 and are rejected for the same reasons.

13. As per Claim 10, Qureshi teaches: The apparatus as claimed in claim 9, wherein a different relationship is maintained between said program counter value and an address of an instruction being executed depending upon whether said instruction decoder is operating in said first mode or said second mode (Paragraph 1, if the

machine is reading data in an order it wasn't intended to be read in, then the program counter will point to the wrong address).

Claims 21 and 32 are substantially similar to Claim 10 and are rejected for the same reasons.

14. As per Claim 11, Qureshi teaches: The apparatus as claimed in claim 8, wherein said at least one program instruction generating different result data values includes a program status register value as an input operand (Paragraph 1, if the machine is reading data in an order it wasn't intended to be read in, everything will generate different results).

Claims 22 and 33 are substantially similar to Claim 11 and are rejected for the same reasons.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 7, 18, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Qureshi, in view of McFarland et al. (USPN 5,781,753, herein McFarland).

17. As per Claim 7, Qureshi teaches an The apparatus as claimed in claim 1, but fails to explicitly teach:

wherein said second instruction set is a variable length instruction set.

Qureshi teaches a system to allow a first and second instruction set to run on the same processor, but does not explicitly teach that the second instruction set is a variable length instruction set. However, McFarland teaches that the x86 architecture, one of the most widely used architectures in PC's, and what made PCs into a mass-market item (Column 2, Lines 9-20), contains variable-length instructions that need to be dealt with when designing a machine to run the architecture (Column 5, Lines 56-65). Given the popularity and wide usage of the x86 processor, and the advantage of using Qureshi's system to allow instruction sets of different formats to function together, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Qureshi's invention into a machine running an x86 architecture, which would make variable-length instructions one of the instruction sets Qureshi deals with. Claims 18 and 29 have similar limitations and are rejected for the same reasons.

(10) Response to Argument

1. Appellants first argument in the brief is that Qureshi does not have an instruction decoder to decode program instructions, and can be operable in both modes as disclosed.

While Appellant has admitted that one could infer that there is an instruction decoder of some sort in Qureshi's CPU, Examiner will take that one step further, and assert that the CPU must have an instruction decoder, because no computer can exist without an instruction decoder. Data, both instructions and non-instructions, are a garbled mess of ones and zeros as far as a computer is concerned, until a decoder can put them into a proper context, and instruct the computer what to do with those ones and zeros. Examiner refers to the article "Altari 8800", a processor released in 1975, which explains the importance and fundamental necessity of an instruction decoder on Page 2, where it states that "The instruction decoder is the core of the variable-hardware concept. It decodes the instructions and sets up the various registers, gates, etc., in the CPU for proper functioning." Therefore, there is not just an implication of an instruction decoder in Qureshi, it is an absolute necessity. Furthermore, since Qureshi operates in two modes (As seen in Paragraph 4, operating in little endian mode, or big endian mode), the instruction decoder clearly must operate in both modes, otherwise Qureshi would logically not be capable of executing instructions in both modes. Therefore, because Qureshi functions, and functions in both modes, the conclusion must be that Qureshi teaches an instruction decoder, to decode program instructions, and operable in both the disclosed modes in Qureshi. To look at Qureshi from the Appellant's interpretation, that is, that this instruction decoder does not exist, Qureshi would not be capable of functioning, which is clearly not a valid interpretation of the reference.

2. Appellant further argues that Qureshi does not teach the claimed first and second instruction sets, because Qureshi teaches that the two modes are the same instruction set, stored in different formats.

However, as explained earlier in the Examiners claim construction, there is absolutely no indication, implicit or explicit, that the first and second instruction sets claimed are distinct from each other. It would be improper of the Examiner to immediately assume that they are different, because to do so would be to improperly bring in Appellant's specification into the claims. The Examiner is required to make the broadest reasonable interpretation of the claims, as set forth by the MPEP, and the broadest reasonable interpretation is that the first and second instruction sets could be different, but they could also be the same. Since Qureshi reads on the claims when the instruction sets were the same, Examiner applied the art to the claims.

3. Appellant further argues that Qureshi lacks the claimed subset of program instructions, having a common bit length and common storage order compensated encoding, such that after compensating for storage order differences, all bits are identical.

Appellant is correct in that Examiner is suggesting that the first and second subsets are the same. Despite Appellants arguments that the terms “first” and "second" is to distinguish between multiple, distinct features, this is not the meaning of the terms. As explained above in the claim construction section, “first” and “second” are merely identifiers. One can claim a first barrel and a second barrel, and they may both contain

apples, one may contain apples and one may contain oranges, or both could contain oranges. The words "first" and "second" mean absolutely nothing in regards to what is the content of the object they describe. It would be unreasonable, and improper, of the Examiner to read the Appellant's specification into the claims, given that Appellant has provided absolutely no definition, in either the specification or the claims, to indicate that the first and second subsets are different sets. While Appellant appears to find this reasoning unreasonable and contrived (as stated in Page 12), it does not change the fact that it is not proper to make the interpretation the Appellant is arguing, and if the Appellant intended to claim two different subsets, the Appellant should have made some indication that the sets were different, but they declined to do so, and as a result, the Examiner must make the broadest reasonable interpretation of the claim, which is that the claims must not only encompass the possibility of the subsets being different, but that it also encompasses the possibility that they are the same. To do any less would be to improperly apply the Appellant's specification to the claims.

4. Appellant has additionally argued that Qureshi lacks the "common subset of instructions", as Examiner position the limitations have been read, as argued that the two subsets comprise the same set, which Appellant has correctly argued that this would "imply that the two instruction sets are the same, which has been established above. Appellant has argued that there would be no need for an instruction decoder which is operable in both a first mode, and a second mode, if the instruction sets were the same, however, this is clearly not correct, as the modes determine in what storage

format the data and instructions are stored in, as taught by both Qureshi and the Appellant. The claims would certainly not be meaningless, because what is being claimed is what is taught in Qureshi, that in the first mode, the instructions are stored in big endian format, and in the second mode, the instructions are stored in little endian format. When all storage order differences are accounted for, all bits are identical. This is exactly the invention of Qureshi, so clearly, the claim language is not meaningless, since it corresponds directly to another invention, the invention which was applied as prior art to the claims.

5. Regarding Appellant's arguments for Claims 2, 13, and 24, Examiner refers to the previous remarks, which explain both why an instruction decoder must be in the system, and how it decodes both instruction sets.

6. Regarding Appellants arguments for Claims 3, 14, and 25, Examiner refers to Paragraph 17, which show that multiple CPUs may be in the system of Qureshi, thus co-processors, and anything that executes on a co-processor thus is a co-processor instruction. The same remarks apply to the arguments for Claims 4, 8, 15, 19, 26, and 30.

7. Finally, in regards to Appellants arguments for the remaining claims rejected under 102, the Examiners reasoning about reading data out of order is completely relevant to the claims, as one of skill in the art would recognize. A program counter is an

essential input for all instructions, because the program counter determines which instructions execute in what order, and one would recognize that not only is a program counter required in all computers, but is also necessary as an input operand to ensure that instructions are not executed randomly. Therefore, Examiner asserts that his rejection did address the claims, and is relevant, and one of skill in the art would recognize this as such, and to assert otherwise would require evidence to show a computer that can execute instructions without an indication of what instruction is supposed to be executed, which logically does not make a great deal of sense.

8. Regarding Appellant's arguments for the Claims rejected under 103, Examiner refers to his above remarks, as there is no "confusion" present on the part of the Examiner, as the Appellant has stated on Page 16, but rather, the Appellants repeated attempts to improperly read limitations from the specification into the claims appears to be the basis of the Appellants arguments, which the Examiner has already addressed.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Robert Fennema

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